(e:
- provides low reactance path / ac signal to GND or shunt AC signal away from RE, if not done RE will causes the voltage drop.

- At the input sides of R_1, R_2 and RE forms the biasing ckt for the stabilization of ckt i.e maintains fixed Q-point.

Small Signal Analysis: (a) Input resistance, Rin
(b) Output " , Rout
(c) Voltage gain, AV
(d) current gain, Ai

(a) Rin:. depends upon valve of Freq of vin
. Total equivalent resistance of the i/p Network as seen from i/p terminals

(b) Output Resistance; $R_{out} = \frac{U_x}{I_x} \simeq R_C$

$U_x \rightarrow$ applied voltage at o/p side
$I_x \rightarrow$ current due to equivalent voltage applied.

(c) Voltage gain (Av): $\frac{V_o}{V_{in}}$

(d) current gain (Ai): $\frac{I_o}{I_{in}}$

Ckt Analysis:

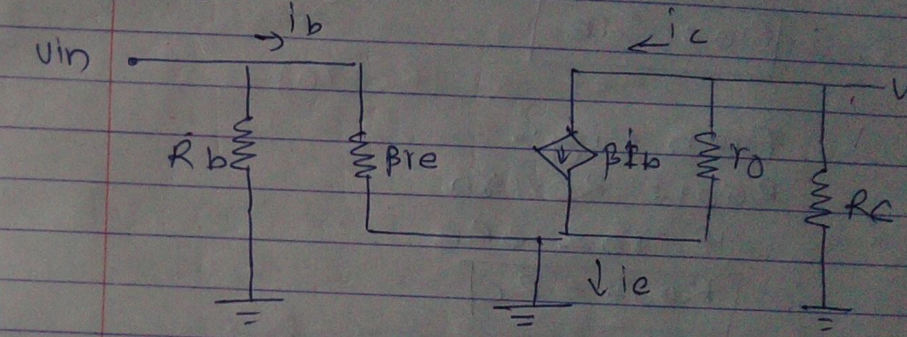


fig: re-model for CE config.

$R_{in} = \frac{V_{in}}{I_{in}}$, $R_{ib} = \frac{V_{ib}}{i_b}$

from fig:

$R_{in} = \frac{V_{in}}{I_{in}}$

And,
$R_{in} = R_b // R_{ib}$

where, $R_b = R_1 // R_2$
R_{ib} = i/p resistance looking into the base since the emitter is GNDed

So, $R_{ib} = \beta r_e = \frac{v_{ib}}{i_b} = \beta r_e$

$R_{in} = R_b \parallel \beta r_e$

Since $R_b \geq 10 \beta r_e$

$$\boxed{R_{in} = \beta r_e}$$

from Fig:-

$R_{out} = R_C \parallel r_o$

If $r_o \geq 10 R_C$

$$\boxed{R_{out} \doteq R_C}$$

finding A_V:

$V_o = i_o \cdot R_{out}$

$= -i_c \cdot R_{out}$

$= -\beta i_b \cdot R_{out}$

Also,

$$i_b = \frac{v_{ib}}{R_{ib}} = \frac{v_{in}}{\beta r_e}$$

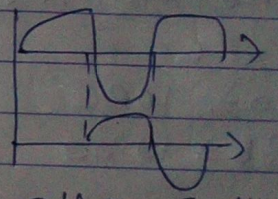
$$\therefore V_o = -\beta \cdot \frac{v_{in}}{\beta r_e} \cdot R_{out} = -\frac{v_{in} R_{out}}{r_e}$$

$$\therefore A_V = \frac{v_o}{v_{in}} = \frac{-v_{in} R_{out}/r_e}{v_{in}} = -\frac{R_{out}}{r_e}$$

$$= \frac{-R_C \parallel r_o}{r_e}$$

$$= -\frac{R_C}{r_e}$$

(-ve ~~ind~~ sign indicate that signal is out of phase by 180°)



Note: It is also called No load voltage gain (A_{VNL}) $= \frac{R_C}{r_e}$

Finding A_i;

We have;

$$A_i = \frac{i_o}{i_{in}} = \frac{i_{out}}{i_b} * \frac{i_b}{i_{in}}$$

using current divider rule,

$$i_{out} = -\beta i_b \left(\frac{r_o}{R_C + r_o}\right)$$

$$i_b = i_{in} \left(\frac{R_b}{R_b + R_{ib}}\right) = i_{in} \frac{R_b}{R_b + \beta r_e}$$

$$A_i = \frac{-\beta i_b \left(\frac{r_o}{R_c + r_o}\right)}{\frac{i_b (R_b + \beta r_e)}{R_b}}$$

$$= -\beta i_b \left(\frac{r_o}{R_c + r_o}\right) * \frac{R_b}{i_b (R_b + \beta r_e)}$$

$$= -\frac{\beta R_b r_o}{(R_b + \beta r_e)(R_c + r_o)}$$

if $r_o \geq 10 R_c$

$R_b \geq 10 \beta r_e$

$$A_i = \frac{-\beta R_b r_o}{\beta o \, R_b} = -\beta$$

Effect of source resistor (R_S) and load R_L

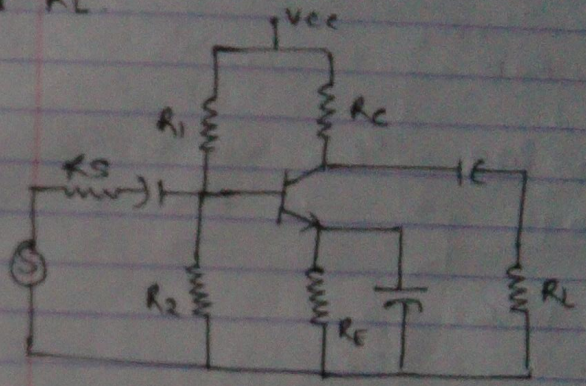


fig: CE Amplifier ckt with some source resistance (R_S) and load resistance (R_L)

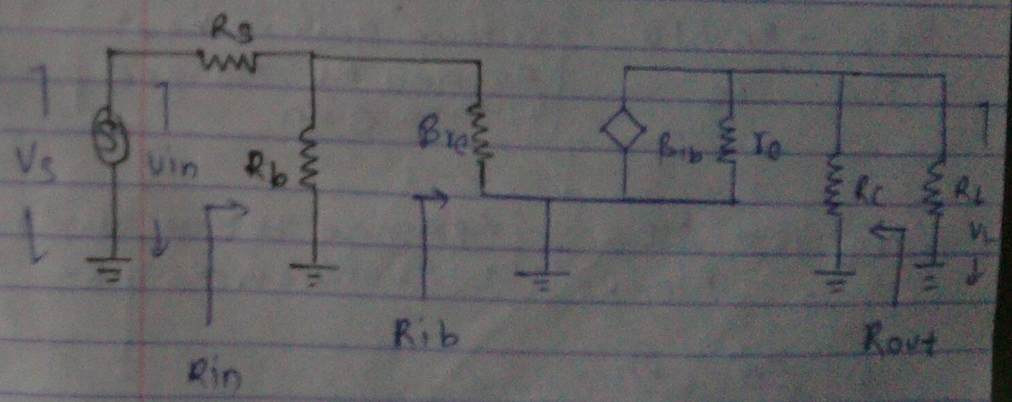


fig: Small Signal re model

finding Rin;

$R_{in} = R_b // R_{ib}$

$\therefore R_{in} \cong \beta r_e$

finding Rout;

$R_{out} \cong R_c$

finding AVS;

$$A_{VS} = \frac{V_L}{V_S} = \frac{V_L}{V_o} * \frac{V_o}{V_{in}} * \frac{V_{in}}{V_S} \quad \text{— (a)}$$

$\frac{V_o}{V_{in}} = \frac{-R_c // r_o}{r_e}$ [Voltage gain without Rs and RL No load voltage gain]

$V_{in} = V_s * \frac{R_{in}}{R_{in}+R_s}$ [Applying voltage divider rule between Rs & Rin]

$\therefore \Rightarrow \frac{V_{in}}{V_s} = \frac{R_{in}}{R_{in}+R_s}$

similarly at the o/p applying voltage divider rule, between Rc & RL

$V_L = \frac{R_L}{R_L + R_{out}} * V_{out}$

$\frac{V_L}{V_o} = \frac{R_L}{R_L + R_{out}}$

Replacing values at (a)

$$A_{VS} = \frac{R_L}{R_L + R_{out}} * \frac{-R_c // r_o}{r_e} * \frac{R_{in}}{R_{in}+R_s}$$

$$= \frac{R_L}{R_L + R_{out}} \cdot (A_{Vo}) \cdot \frac{R_{in}}{R_{in}+R_s}$$

where, A_{Vo} = voltage gain without load (A_{VNL})

Bode-plot of frequency Response

Since the voltage gain, $A_V = \frac{1}{1 - j(f_1/f)}$

$$|A_V| = \frac{1}{\sqrt{1 + (f_1/f)^2}}$$

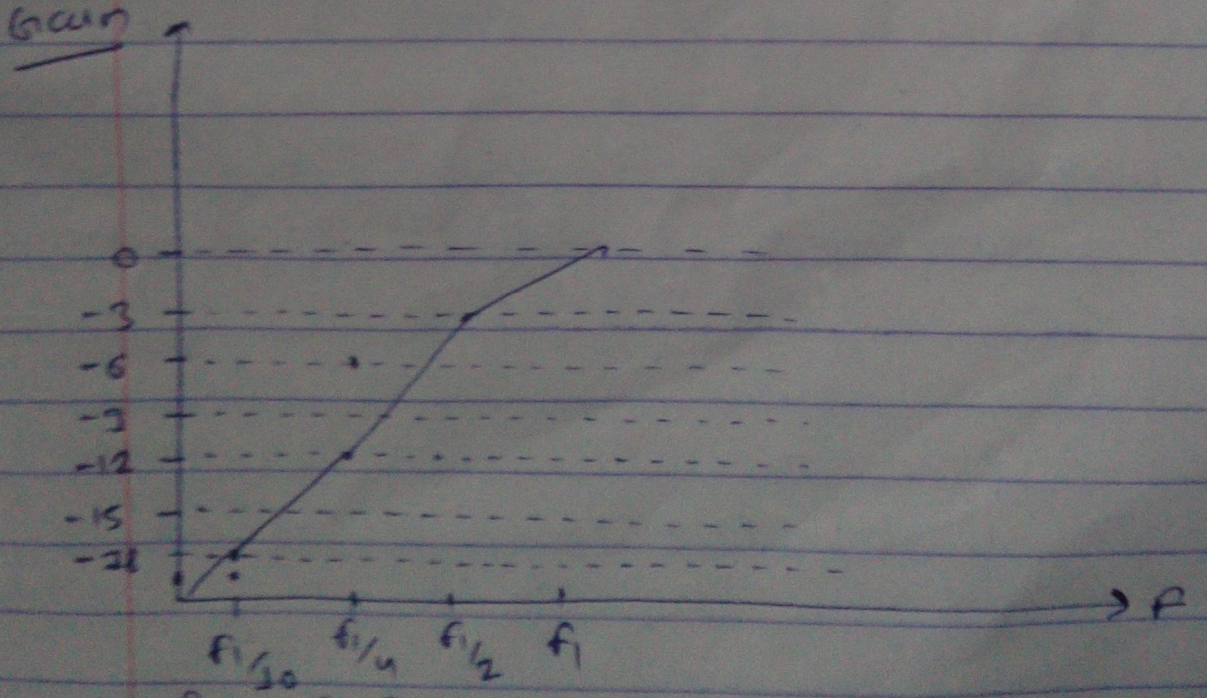
In DB

$$20\log_{10}(A_V) = |A_V|_{dB}$$

$$20\log_{10}(A_V)_{dB} = 20\log_{10}\left[\frac{1}{\sqrt{1 + (f_1/f)^2}}\right]$$

$$= -10\log\left(\frac{f_1}{f}\right)^2$$

$$= -20\log\left(\frac{f_1}{f_2}\right)$$



for $f = f_1$, $|A_V|_{dB} = 0dB$

$f = f_1/2$; $|A_v|_{dB} = 6.02 \approx 6\,dB$

$f = f_1/4$; $|A_v|_{dB} = -12\,dB$

$f = f_1/10$; $|A_v|_{dB} = -20\,dB$

Review of low frequency AC and DC models:

models:- Equivalent ckt which behaves as the original device
- low loss

Introduction:-

- DC Analysis (large signal model)
- AC Analysis (small signal model)

DC Analysis:

purpose to find the Q-point (operating point) of the amplifier ckt:

for this:

1) We reduce all the ac sources to zero ie ac voltage source are replaced by short ckt and AC current source are replaced by open ckt.

2) Open all the capacitor (if any) Because they BLOCK DC, to observe effect of transistor.

AC Analysis:

1. DC Analysis should be done, inorder to find Q-point, AC input signal source are applied. for AC Analysis only AC signal

consider making all DC source zeros.
for this:

- Reduce all the DC-sources zero and replacing them by a short ckt equivalent.
- Replace all capacitor (if any) by a short ckt equivalent.
- We replace the transistor with its small signal equivalent ckt

The important parameters to be determined in case of transistor or amplifier prior to analysis:

1. Voltage Gain:

$$A_V = \frac{V_o}{V_{in}}$$

2. Current Gain:

$$A_i = \frac{I_o}{I_{in}}$$

3. Input impedance:

$$Z_{in} = \frac{V_{in}}{I_{in}}$$

4. Output impedance.

$$Z_o = \frac{V_o}{I_o}$$

- The re-model of BJT (small signal model)

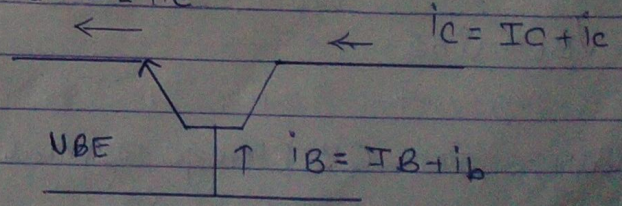
The re model uses transistor, Beta and reverse valves. This model is popular because of the following advantages:

1. The required parameters are easily available.
2. Simple and easy procedure.
3. Result obtained have a fairly good accuracy for the study of characteristics of amplifier ckt.

However the re-models fails to account for the output impedance level of the device and the feedback effect from output to input

- Common base configuration:

(Electrical equivalent models for CB config)



Since BE Junction is forward Biased and C-B Junction is reversed biased. The ac i/p signal which is to be applied is supper imposed on bias voltage of the i/p ckt.

from fig:

$$i_B = I_B + i_b \quad -(1)$$
dc ac

Similarly,

$$i_E = I_E + i_e \quad -(2)$$

And $i_C = I_C + i_c \quad -(3)$

$$\alpha_{dc} = \frac{I_C}{I_E}, \quad \alpha_{ac} = \frac{i_c}{i_e}$$

for simplicity,

$\alpha_{dc} = \alpha_{ac}$

$$V_{BE} = V_{BE} + V_{be}$$

(a) DC-Analysis for CB (large signal analysis)

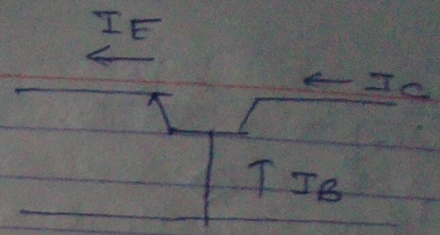


fig: DC- component Acting alone in CB configuration.

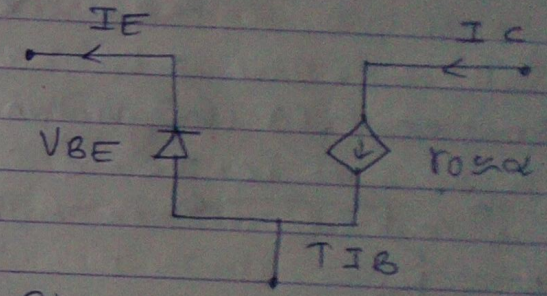


fig: DC- model diode

(b) AC analysis of CB (re-model)

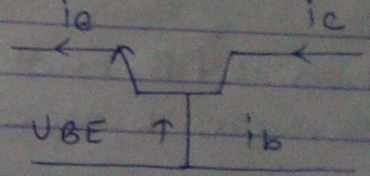


fig: AC component acting alone in CB configuration

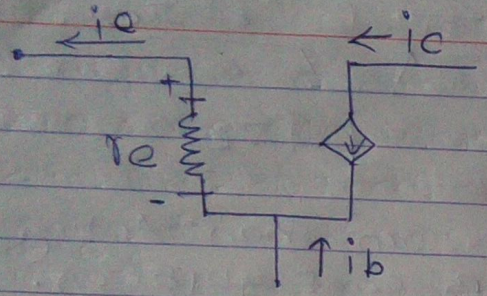


fig: re-model for CB.

- Common Emitter (CE) configuration.

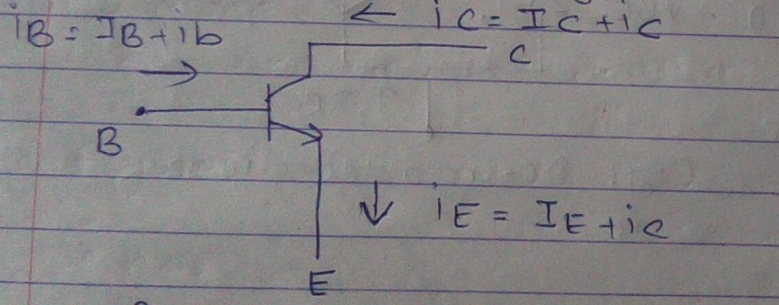


fig: CE BJT transiter

BE Junction is fB and CE Junc-tion is revesed biased.

Base current, iB = IB + ib
Similarly, ic = Ic + ic
iE = IE + ie

Also for CE configuration;

$\beta_{dc} = \frac{I_C}{I_B}$

$\beta_{ac} = \frac{i_c}{i_b}$

for simplicity,

$\beta_{dc} = \beta_{ac}$

Again; $v_{BE} = V_{BE} + v_{be}$

$v_{CE} = V_{CE} + v_{ce}$

(a) DC analysis for CE config:

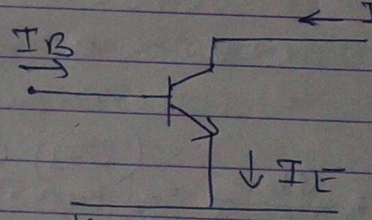


fig: dc component Acting alone.

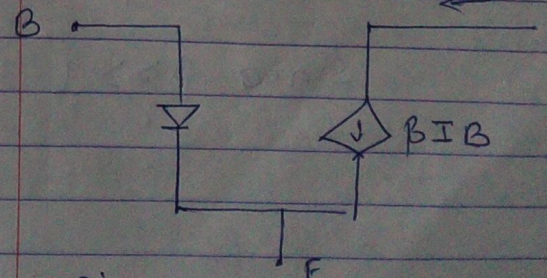


fig: dc-model / Diode model

(b) AC Analysis and small signal model

Here we consider only ac signals and remove all dc-component.

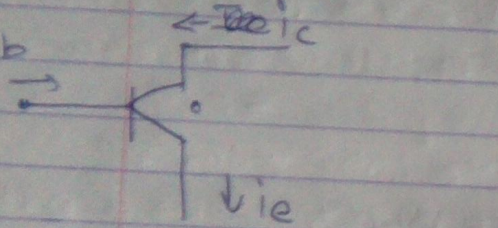


fig. AC component acting alone

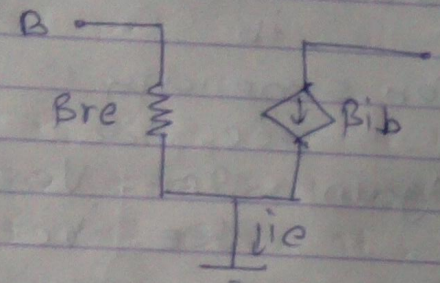


fig: re-model

from figure;

We have,

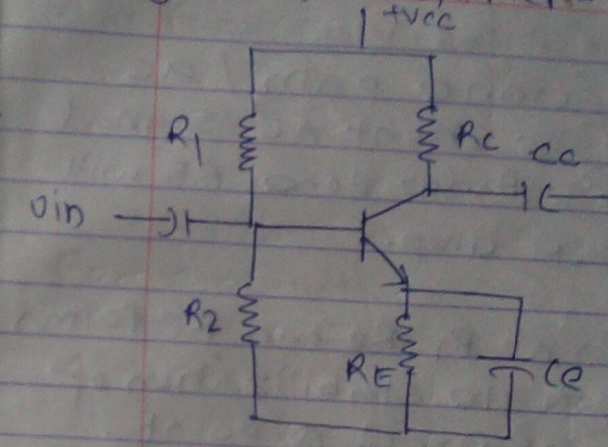
$$r_{in} = \frac{v_{be}}{i_b} = \frac{v_{be}}{\frac{i_e}{\beta+1}} = (\beta+1)\frac{v_{be}}{i_e}$$

$$= (\beta+1) r_e$$

$$= \beta r_e$$

Since $\beta >> 1$

Single stage Amplifier:-



Cc ⇒ coupling capacitor

fig: CE amplifier ckt with emitter bypass capacitor CE.

Cc: • Isolates dc signal of one stage to another

• Act as perfect short ckt while blocking dc

• Couples one stage of amplification to next stage.

• If not use Q-point of next stage changes drastically due to effect of $R_C // R_1$ of next stage.

$R_C // R_1$ is called shunting effect or loading effect.